

# **Epitaxy for Physics Research and Device Applications:**

and other Research activities in the Semiconductor Materials Research Laboratory

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# Epitaxy of Semiconductors for Physics Research and Device Applications

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### Fundamentals of Epitaxy





# 2D Electron System in Strained Si

in collaboration with D.C. Tsui & group, Princeton University

Other collaborations: Marc Kastner (MIT); Jagadeesh Moodera (MIT magnet lab)

- The compositionally graded, relaxed SiGe buffer layers: the controlled plastic relaxation of misfit strain that forms the foundation for the fabrication of strained Si;
- The magnitude of strain required for effective separation between the 2- & 4-fold conduction band valleys: ~1%;



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#### Modulation Doped 2DES





The "Usefulness" of 2-dimensional Electron Systems in Strained Si

- Room T applications:
  - Mobility being limited by phonon scattering;
  - High carrier density: the need for large current drive;
  - The importance of the out of plane effective mass;
- Low T transport research:
  - High mobility: fine features in the transport characteristics;
  - Low carrier density: the importance for correlated behaviors;
  - Application: topological quantum computing?
  - Understanding correlated electron behaviors is at the forefront of condensed matter physics;





A machine based on bizarre particles called anyons that represents a calculation as a set of braids in spacetime might be a shortcut to practical quantum computation

Scientific American, p.56, April 2006,

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## Integer Quantum Hall Effect: electron localization



The density of state increases and the 2D electrons pack closer together with increasing B

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## Fractional Quantum Hall Effect: Composite Fermions



J.P. Eisenstein, et al, Phys E, v.6, 29 (2000)

The details of the  $\rho_{xx}$ -B relation can be visible only if the mobility is high; Fractional quantum Hall effect: the need to invoke correlated electron behaviors  $S_{emiconductor} M_{aterials} R_{esearch} L_{ab}$ 



The in-ability of resolving fine features in the transport ( $R_{xx} \& R_{yy}$ ) curves because of low  $\mu$ .





• The importance of low carrier density for the study of correlated behaviors:

The dimensionless density parameter:

 $r_s = E_{e-e}/E_F$ 

Given that  $E_{e-e} \sim \sqrt{(n_s)}/\epsilon$  and  $E_F \sim n_s/m^*$ , where  $n_s$  =carrier density,  $\epsilon$ =dielectric constant and m\*=effective mass.

Therefore:

 $r_s \sim m^* / \epsilon \sqrt{(n_s)}$ 

To achieve large  $r_s$ , we need large m<sup>\*</sup>, and small  $n_s$ .



- The factors that could limit the achievable carrier density;
  - Localization induced by impurities and other inhomogeneity in the sample;
  - The uniqueness of 2DES in strained Si: another source for poor homogeneity.





## The Challenges in Achieving Low 2DES Density

Raman Mapping of SSOI (Mark Kennard, SOITEC)



Misfit dislocation

Si substrate

**Deformation potential calculation** 



Amplitude of potential undulation: 7 meV Spatial correlation: ~1 um; Lower limit of carrier density : 5~6x10<sup>10</sup>cm<sup>-2</sup>

Alternatives: avoid dislocation

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# An alternative method for fabricating dislocation-free strained Si





## An alternative method for fabricating dislocation-free strained Si



Dislocation-free 100nm thick Si film under 1% tension with strain variation undetectable by Raman

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- Sample fabrication (the enabling factor): The continued quest for 2-D electron or hole systems with higher mobility and/at carrier density.
- Physics: 2-D electron and hole systems with increasingly complex energy band structures that allows the probing into the complex world of correlated behaviors.

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## and other Epitaxy related Research activities in the Semiconductor Materials Research Laboratory

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# Dark-field Transmission Electron Micrographs of GaN on Sapphire



YHX February 2008



# Scalable Silicon Tunnel Transistor Technology for Low Power Circuits (S2T3)

#### DARPA STEEP Program

#### Jason Woo, PI, EE UCLA



#### Requirements:

- Carrier concentration as high as possible;
- Abrupt doping concentration gradient.

#### Materials science challenge:

• High dopant concentration while maintaining 100% in substitutional sites;

• Minimize diffusion while maintaining "good" crystalline quality in terms of point defects.

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# HRTEM of Ge Spikes Separated by 1 nm Si on Si (001)



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## Pushing the Limit on the Abruptness of Compositional Transition collaboration with Intel @ Oregon





# The rise of graphene

Jason Woo, PI, EE UCLA



A. K. Geiml and K. S. Novoselov, Nature Materials 6, 183 - 191 (2007)

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## and other Non-epitaxy Research activities in the Semiconductor Materials Research Laboratory

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# Understanding the Scaling Limit of PcRAM Technology of Chalcogenide Materials



A.L. Lacaita / Solid-State Electronics 50 (2006) 24–31, Phys. Rev. Lett. 96, 055507 (2006)

<u>Characteristic features</u>: significant difference in optical and electrical properties between amorphous and poly-crystalline states.

From optical memory to electronic memory: the size of the programming volume.

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- 1. The minimum size required for the existence of 3 distinguishable phases in chalcogenide materials (amorphous, FCC, and HCP);
- 2. The phase change kinetics as a function of the volume: the effects of interface and surface;
- 3. The cross-over from nucleation dominated crystallization process to growth dominated regime with reducing volume;
- 4. Assessment of thermal proximity effect and the implication on technology scaling limit.

Work in progress

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Nano-Patterning: the prerequisite for our research



5.0kV 3.4mm x301k SE(U) 5/18/2007

100nm



Nano-Patterning: the prerequisite for our research



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# A Quantum Dot Based Electro-optic Modulator

for chip-to-chip optical interconnects

- The non-zero R, L, and C in each real electrical wire;
- For high frequency or bit rate, electrical interconnects are prone to data skew and crosstalk with an ultimate bit rate limit:  $B \approx \frac{A}{l^2} \times 10^{15} (bps)$
- The rate limit B is determined by the aspect ratio of the interconnects and is <1 Gbps for typical chip interconnect geometry;



"Limit to the bit-rate capacity of electrical interconnects from the aspect ratio of the system architecture", D.A.B. Miller and H.M. Ozaktas, J. Paral. Distrib. Comput., v.41, 42 (1997). Semiconductor Materials Research Lab



# Schematics of Our Quantum Dot Based Modulator Structure

• Using **semiconductor quantum dots** operating near <u>saturation absorption</u> as the electro-absorption medium;

• Employing a dielectric vertical cavity for signal (both the pumping light intensity and the modulation effect) amplification;

- A capacitor as opposed to a current injection device from the circuit perspective;
- Inherently compatible with 2D array architecture.





## Quantum Dot Absorption under External Electric Field

#### Saturation absorption of QDs





# RF Crosstalk Isolation Technology Substrate impedance engineering





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