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Printed Graphene Circuits**

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A single layer of graphite, graphene,[1,2] is a truly 2-dimensional semi-metallic material composed of only one atomic layer of carbon atoms. Graphene's peculiar band structure suppresses carrier backscattering, leading to extremely high carrier mobility.[2] Narrow graphene ribbons are predicted to have a semiconducting energy gap tunable by width,[3] indicating a path to device fabrication. In addition, because graphene is only one atom in thickness, transport properties are expected to be sensitively influenced by atomic scale defects, adsorbates,[4,5] local electronic environment, and mechanical deformations; consequently, graphene is a promising sensor material. To date, graphene has been obtained by only two methods: mechanical exfoliation of graphite on SiO_2/Si[1] or thermal graphitization of a silicon carbide (SiC) surface.[2] In each case, the substrate strongly influences the graphene properties; charge defects in SiO_2 are thought to limit the mobility, and strong interaction with SiC introduces a large charge density. Furthermore, the substrate can limit the graphene device possibilities; gating of devices on SiC is difficult, and on SiO_2/Si the presence of a conducting backplane (also used as the gate) precludes high-frequency device operation. In this paper, we report the transfer of graphene from one substrate to another to realize flexible, transparent graphene devices with high field effect mobility. This represents the ultimate extension of printing technology to a single atomic layer.

We employ the transfer printing method[6,7] to transfer graphene between SiO_2/Si and plastic substrates, as well as to assemble the gate dielectric, and source, drain, and gate electrodes, forming a complete graphene field-effect transistor with local gate on a flexible, transparent substrate. Transfer printing enables device component fabrication and assembly to be performed separately, and has found wide application in printed circuits and flexible electronics research.[7–10] By properly tuning the adhesion of the printed material to the original and target substrate,[7] our technique can in principle enable the transfer of graphene to *any* substrate, thus greatly expanding the possible applications of this material.

Figure 1a–c depicts the basic process required to print a patterned layer of material from one substrate (the transfer substrate) over to a second substrate (a PET plastic substrate). The devices require three process steps performed sequentially to assemble (1) source-drain electrodes, (2) graphene, and (3) gate electrode/dielectric. First, photolithography is used to prepare 30 nm thick Au source and drain electrodes on a silicon wafer with an oxidized surface (SiO_2/Si). The electrodes are then transferred onto the PET substrate as described elsewhere.[6,7] Then, single- and few-layer graphene is obtained from Kish graphite by mechanical exfoliation[1] on 300 nm thermally-grown silicon dioxide on silicon substrates, and its thickness and morphology characterized by atomic force microscopy. Mechanical exfoliation yields atomically-clean graphene sheets[11,12] and our AFM images also indicate that the graphene sheet is free of nanometer-scale contaminants. In addition, chemical contamination caused by exposure to photoresist and lift-off chemicals is avoided in this process. The desired graphene sheet is printed at 170 °C at 500 psi from the SiO_2/Si to the source-drain electrode assembly on PET. Under these conditions, the PET substrate is above its glass transition temperature, and can conform to the transfer substrate morphology.[7] Finally, the gate assembly consisting of a photolithographically patterned 100 nm Au gate electrode and a 600 nm thick poly(methyl methacrylate) (PMMA) gate dielectric is prepared on SiO_2/Si and transfer printed onto the device substrate at 175 °C at 500 psi. Each subsequent layer is aligned optically to the pre-existing features. Figure 1d shows the schematic of a completed device. An advantage of this method is that it exposes graphene to no chemicals used in conventional lithography processes, by which most of the graphene devices on silicon dioxide are fabricated. Lithography processes have been found to leave resi-

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ADVANCED MATERIALS

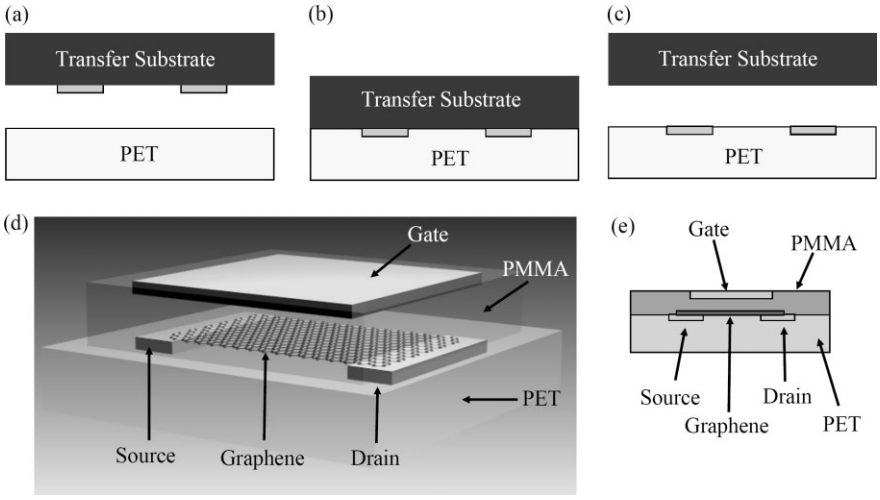

Figure 1. a)–c) Printing procedure used to print a feature layer. a) The desired features, e.g., two gold electrodes, are predefined on the transfer substrate. b) The transfer substrate is brought into contact with the plastic substrate at an elevated temperature and high pressure. Temperature and pressure are optimized to ensure successful transfers. c) The transfer substrate is removed from the plastic substrate, leaving the features embedded in the plastic substrate. The process may be repeated to assemble additional components. d) The 3D schematic and e) the cross sectional view of the completed graphene device, not drawn to scale.

due on the device[12] and might negatively influence transport properties.

The printing process is successful in transferring graphene materials, ranging from monolayer sheets to bulk graphite, from the silicon dioxide substrate to PET and Au. Figure 2a shows an optical microscopy image of a graphite film with thicknesses from monolayer to multilayer on a silicon dioxide substrate. Figure 2b shows the graphene material printed to the source-drain electrodes on PET (the image is reversed to aid comparison to Fig. 2a). By comparison of Figure 2a and b, it is clear that the conduction from source to drain electrode takes place through the portions labeled "monolayer" and "bilayer" in Figure 2a, in series. (As a visual aid, red dotted lines have been added to Fig. 2a as an indicator of the location of the edges of the source-drain electrodes (separated by 6 μm) with respect to the graphene before printing.) The thickness of the monolayer portion is confirmed by atomic force microscopy (AFM) before transfer printing as shown in Figure 2c and d. Figure 2c is an AFM micrograph acquired in the boxed region indicated in Figure 2a, which shows the functioning monolayer portion with another monolayer lying across it. The red box in Figure 2c shows an area where the top layer steps down from the functioning layer to the substrate, and the step height here is the thickness of the functioning layer. Figure 2d shows the height histogram of the area inside the black box in Figure 2c. Fitting the histogram by two Gaussian peaks gives an estimate of the thickness of the monolayer portion to be (3.95 ± 0.09) Å, which confirms that the functioning material is single layer graphene.[12]

After transfer no graphene is observed in optical images on the silicon dioxide substrate; this indicates that graphene adheres more strongly to PET and Au than to the original silicon dioxide substrate, and the interlayer coupling strength of graphite is stronger than its adhesion to the silicon dioxide surface. The presence of the Au source-drain electrodes is not necessary for transfer of graphene materials from silicon dioxide substrates to PET; graphene materials can be transferred to bare PET, as suggested by simulations.[13] Graphene materials are barely visible once transferred onto PET as seen in Figure 2b, and can only just be discerned on the source-drain electrodes. Graphene is nearly completely transparent at visible wavelengths.

Measurement of the transport properties is important to assess the usefulness of the transfer printing process. Figure 3a shows the room temperature conductivity[14] as a function of gate voltage $\sigma(V_g)$ of the "printed" device shown in Figure 2b. As seen in Figure 2a and b, this device consists of two portions (monolayer and bilayer) in series. As graphene sheets are semi-metals with linearly vanishing electronic densities of states at the charge-neutral point, the applied gate voltage modifies the conductivity. The slope of the linear portion of the transfer curve is used to calculate the field effect mobility, $\mu = \frac{1}{c_g}\frac{d\sigma}{dV_g}$, where c_g is the gate capacitance per unit area (4.4 nF cm^{-2}). This particular device shows a maximum field effect mobility of 1.0×10^4 cm^2 V^{-1} s^{-1} for holes and 4×10^3 cm^2 V^{-1} s^{-1} for electrons. Another device composed solely of a monolayer material showed similar field effect mobilities. These values are comparable to the best field effect mobilities measured for graphene devices on SiO_2 at room temperature, for example 2×10^3–5×10^3 cm^2 V^{-1} s^{-1} reported by Novoselov et al.,[1] and 2×10^3–1.5×10^4 cm^2 V^{-1} s^{-1} reported by Tan et al.,[15] suggesting that the transfer method does not damage the graphene and no chemical bonding was established between graphene and plastic substrates.

The minimum conductivity for the "printed" graphene device, shown in Figure 3 is approximately 0.6 mS or $\approx 8G_0$, where $G_0 = \frac{2e^2}{h}$ is the quantum of conductance. The minimum conductivity reported for monolayer[16] and bilayer[17] graphene-based devices is often near $2G_0$ (but may be higher in clean samples[18]). The high value of the minimum conductivity for the printed devices indicates that the contact resistance is small in the transfer-printed devices. Overall, the results show that transfer printing graphene can yield electronic devices equaling the performance of the conventional silicon dioxide-supported devices.

The Dirac neutral point of the printed device (see Fig. 3) is about 21 V (a second printed single layer graphene device

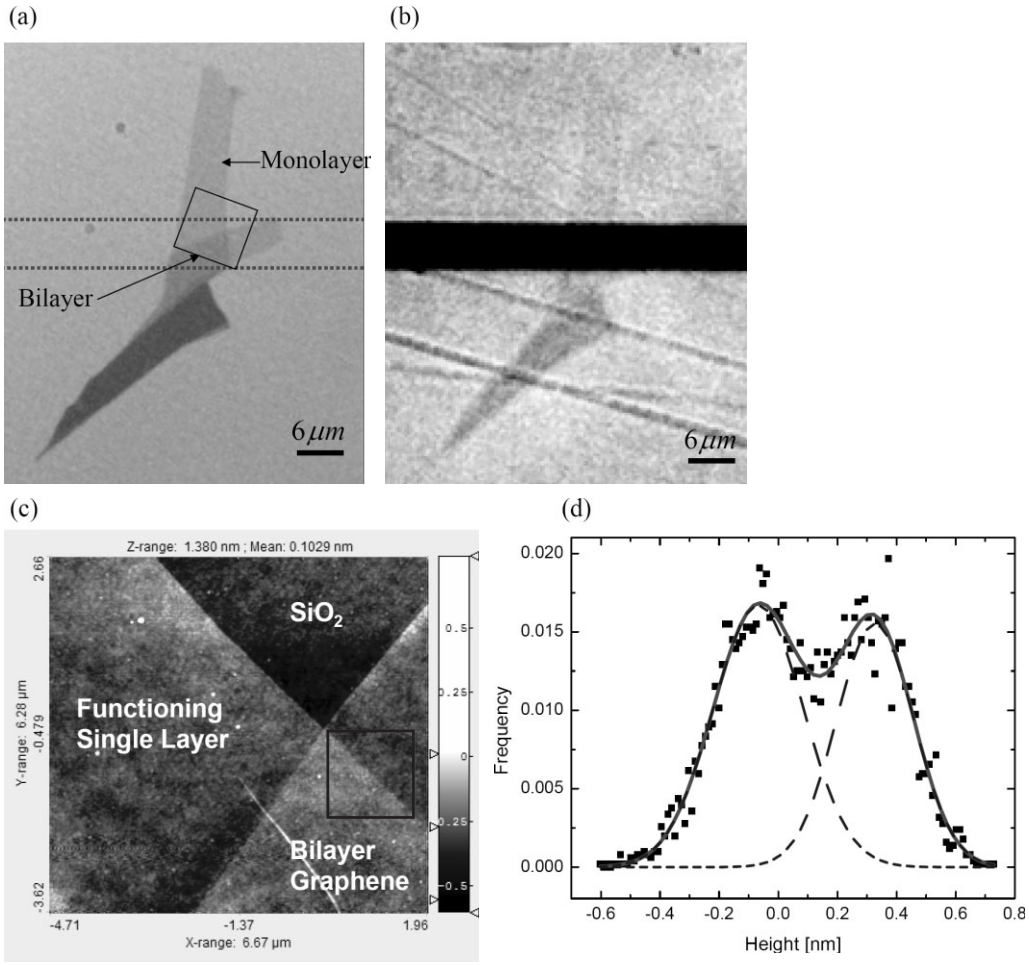

Figure 2. a) Optical microscopy image of a mixed monolayer and multilayer graphene material on silicon dioxide substrate. b) Optical microscopy image of the same graphene sample transfer printed onto the source/drain electrode assembly (dark area is PET, light-gray areas are Au electrodes). The Au source-drain electrodes are bridged by graphene composed of a single-layer portion and a bilayer portion. Note: (b) is left-right reversed to aid comparison to (a). c) Atomic force micrograph of the over lapping area of the sample in (a), used to determine the number of graphene layers. d) Histogram of the selected area (area inside the black box) is fitted by two Gaussian peaks. The height difference between the two peaks is (3.95 ± 0.09) Å, which indicates that the functioning material is single layer graphene.

showed the same shift), which corresponds to net positive charge density of 5.8×10^{11} cm^{-2}. One possible explanation is that this shift originates from excess positive trapped charge in the polymer substrate.[19–22] The same amount of charge density would be induced by applying 8 V of gate voltage on 300 nm silicon dioxide dielectric. A shift of this magnitude is not uncommon in graphene devices on silicon dioxide,[23] but smaller values have been reported.[24] For comparison, the density of charge traps has been reported to be 2×10^{11} cm^{-2} in PET,[20,22] 5×10^{8} cm^{-2} in PMMA,[19,21] and 5×10^{11} cm^{-2} in thermally grown silicon dioxide.[25] If the Dirac point shift is predominately determined by trapped charge, these observations would suggest that the PET/PMMA sandwich creates an excess of positive trapped charge and a net charge density comparable to the best observed devices on SiO_2. Alternatively, other mechanisms such as a surface dipole moment, work-function difference between graphene and gate, or chemical doping may also be involved.

Finally, electronic[5,18,26] and structural[12] disorder imposed by the substrate, are expected to determine the graphene transport properties, including the mobility, minimum conductivity, and the shift of the Dirac point. The PET/PMMA sandwich substrates in the printed devices nominally[19–22,25] have net trap densities similar to silicon dioxide substrates. The RMS roughness of the substrate is larger for the PET substrates (1.2 nm in a 5 μm × 5 μm area) than for the silicon dioxide substrates (0.25 nm in a 5 μm × 5 μm area). There are two anomalous features in the transport measurements. First, the minimum conductivity is unusually high at $8G_0$ even for the solely monolayer printed devices. This indicates that the reported universality[16] of the minimum conductivity at $2G_0$ is not correct, and the $2G_0$ value may be specific only to certain silicon dioxide-supported devices. In addition, the devices on the plastic substrates always have higher hole mobility (e.g., they do not have electron-hole symmetry). Such asymmetry has not been reported previously for graphene devices.

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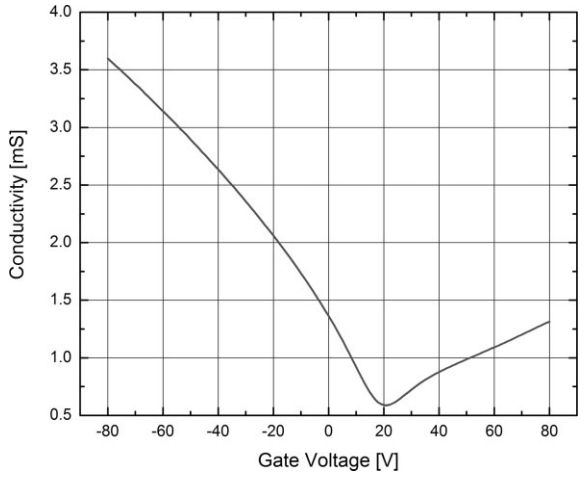

Figure 3. Conductivity as a function of gate voltage for the device in Figure 2b measured at 297 K. The minimum conductivity is about 0.6 mS or $8G_0$ at the Dirac neutral point $V_D = 21$ V, where $G_0 = \frac{2e^2}{h}$ is the quantum of conductance. The capacitance of PMMA dielectric used is 4.4 nF cm^{-2}. 21 V applied across the PMMA dielectric induces the same amount of charge density as 8 V across 300 nm silicon dioxide dielectric. Source-drain bias of 10 mV was applied while acquiring the above data.

The present transport theory,[18,26–28] which focuses on short range or long range scatterers to describe the transport properties, is incapable of explaining such a large asymmetry. The roughness of the PET substrate and the observed high mobility of the printed devices suggest either that the graphene morphology plays little role in determining the transport properties, or that the graphene sheet does not closely conform to the underlying PET morphology. Further work correlating the transport characteristics with systematic variation of substrate charge density and roughness is needed to identify the mechanism behind the differences.

The transfer-printed devices represent the first realization of a local electrostatic gate on graphene-on-insulator. Local gating enables the reduction of gate-source capacitance, which is necessary for high-frequency device operation. Local gating can also be used to explore p–n junctions in graphene, which are predicted to have unusual properties,[29–31] and may form the basis of new bipolar transistor devices.[29] In addition, graphene may represent the ultimate transparent electrode; the resistivity of our graphene at high gate voltage is less than 300 Ω/square, while graphene on PET is so transparent as to be nearly undetectable in the optical microscope.

In conclusion, we have fabricated transparent electronic devices based on graphene materials with thickness down to a single atomic layer by the transfer printing method. The resulting printed graphene devices retain high field effect mobility and have low contact resistance. The results show that the transfer printing method is capable of high-quality transfer of graphene materials from silicon dioxide substrates, and the method thus will have wide applications in manipulating and delivering graphene materials to desired substrate and device geometries. Since the method is purely additive, it exposes graphene (or other functional materials) to no chemical preparation or lithographic steps, providing greater experimental control over device environment for reproducibility and for studies of fundamental transport mechanisms. Finally, the transport properties of the graphene devices on the PET substrate demonstrate the non-universality of minimum conductivity and the incompleteness of the current transport theory.

Experimental

Sample Preparation: Graphene samples are obtained from Kish graphite by mechanical exfoliation [1] on 300 nm thermally-grown silicon dioxide on silicon substrates. Their thickness and morphology are characterized by an atomic force microscope (Digital Instruments (R) IIIa) in the ambient environment.

Device Fabrication: The devices require three process steps performed sequentially to assemble (1) source-drain electrodes, (2) graphene, and (3) gate electrode/dielectric. First, photolithography is used to prepare 30 nm thick Au source and drain electrodes on a silicon wafer with an oxidized surface (SiO_2/Si). The electrodes are then transferred onto the PET substrate as described elsewhere [6,7]. The desired graphene sheet is printed at 170 °C at 500 psi from the silicon dioxide substrate to the source-drain electrode assembly on PET. Finally, the gate assembly consisting of a photolithographically patterned 100 nm Au gate electrode and a 600 nm thick poly(methyl methacrylate) (PMMA) gate dielectric is prepared on SiO_2/Si and transfer printed onto the device substrate at 175 °C at 500 psi. Each subsequent layer is optically aligned to the pre-existing features.

Electrical Characterization: The transfer curves are measured using a probe station in the ambient environment. Source-drain bias voltages of 5 mV, 10 mV and 20 mV are used.

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