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Gate tunable giant anisotropic resistance in ultra-thin GaTe

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Anisotropy in crystals arises from different lattice periodicity along different crystallographic directions, and is usually more pronounced in two dimensional (2D) materials. Indeed, in the emerging 2D materials, electrical anisotropy has been one of the recent research focuses. However, key understandings of the in-plane anisotropic resistance in low-symmetry 2D materials, as well as demonstrations of model devices taking advantage of it, have proven difficult. Here, we show that, in few-layered semiconducting GaTe, electrical conductivity anisotropy between **x** and **y** directions of the 2D crystal can be gate tuned from several fold to over 10^3 . This effect is further demonstrated to yield an anisotropic non-volatile memory behavior in ultra-thin GaTe, when equipped with an architecture of van der Waals floating gate. Our findings of gate-tunable giant anisotropic resistance effect pave the way for potential applications in nanoelectronics such as multifunctional directional memories in the 2D limit.

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It is known that when electrically measuring a bulk material, the resulted conductivity may manifest strong directional dependencies^{1,2}. Discrepancy of conductivity along different in-plane directions in layered bulk crystals can sometimes be as large as a few hundreds, which, however, often requires a certain conditions such as the presence of large external magnetic field³. Recently, low-symmetry 2D materials have attracted significant attentions because of the potential applications of in-plane anisotropic nanoelectronics^{4–11}. For example, ultra-thin black phosphorous flake showed an in-plane anisotropic conductance reaching a ratio σ_a/σ_b of ~ 1.5 , which in principle can be a direction-sensitive sensor⁴. ReS₂ was reported to be another candidate for anisotropic 2D field effect transistor, which exhibited a σ_a of almost 10 times the value of σ_b ⁹. Recent studies on GeP and GeAs flakes also showed anisotropic behavior with anisotropic factors of 1.5–2 for their conductance^{10,11}.

To date, in-plane anisotropic factor Γ_a of electrical conductance in 2D materials is yet limited within one order of magnitude under ambient condition. It thus hinders future applications owing to a weak effective conductance difference between directions, and a larger anisotropic factor is highly desired. In this work, we show an observation of giant anisotropic resistance (GAR) behavior in few-layered *p*-type semiconducting GaTe. Among devices measured, the electrical conductivity ratio along *x* and *y* (*x* and *y* are defined in Fig. 1) directions of ultra-thin GaTe reaches an order of 10^3 at gate voltages close to the valence-band maximum (VBM), which can be further gate tuned down to < 10 , upon hole doping. We show detailed analysis and physical understandings on the GAR effect. Based on this, floating gate anisotropic memory with directional multi-level outputs are demonstrated. Moreover, when measuring along fixed direction, the few-layered GaTe floating gate memory (FGM) exhibits On/Off ratio of 10^7 and retention time of 10^5 s, which is by far the

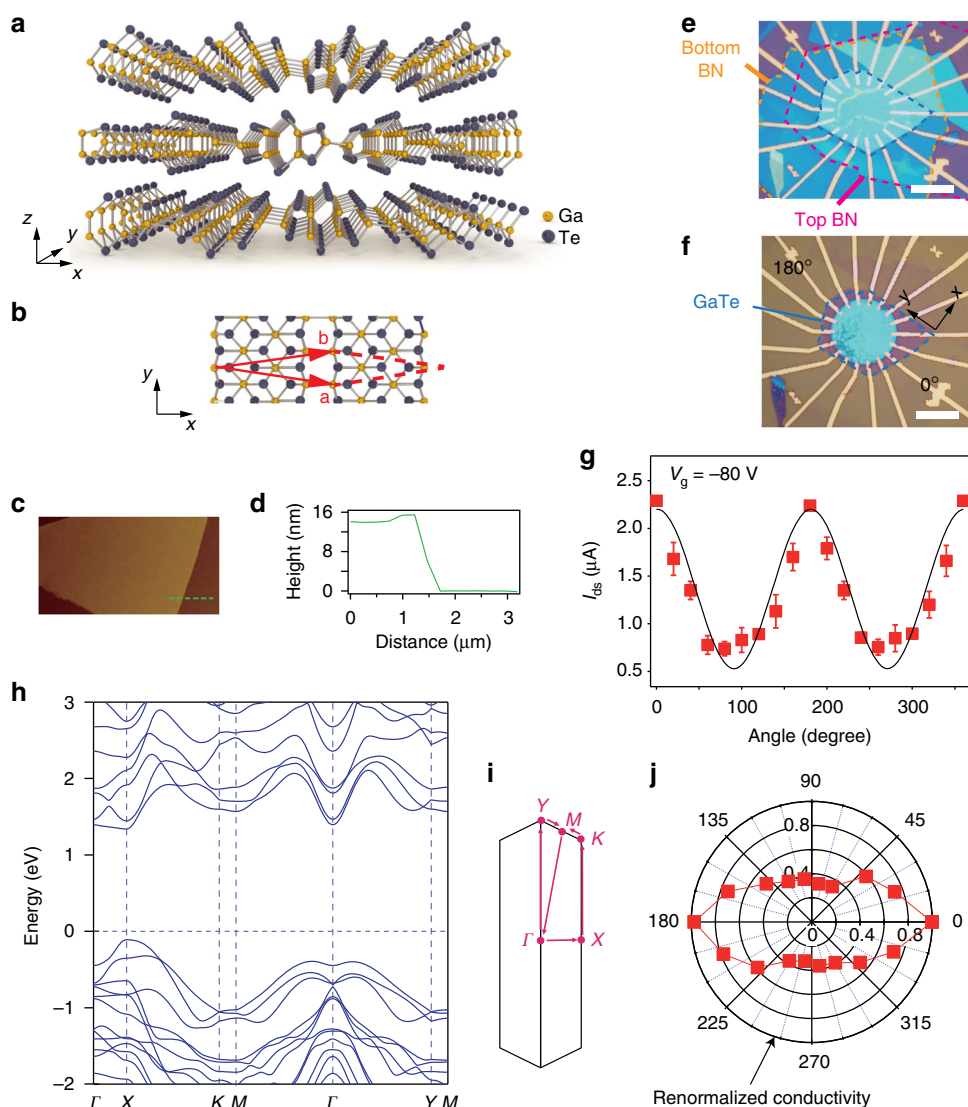


Fig. 1 Characterizations of ultra-thin GaTe. **a** Schematics of GaTe crystal structure, with its in-plane unit cell illustrated in **b**. **c** AFM image of a typical GaTe flake of ~ 14 nm in thickness, with its height profile along the green dashed line plotted in **d**. **e** Optical image of a typical device (sample S1) made of 14 nm GaTe flake encapsulated in h-BN. Electrodes are patterned with an angle interval of 20 degree. **f** Same device in **e** but patterned into a circular shape. Scale bars in **e** and **f** are 10 μm . **g** Source-drain current at $V_{ds} = 2$ V as a function of angle, with $V_g = -80$ V. The black solid line is an ellipsoidal fit. Error bars in **g** are defined as the deviations between experimental data and the fitted line. **h** Electronic band structure of monolayer GaTe, with the first Brillouin zone plotted in **i**. **j** Same data in **g** plotted after re-normalization in a polar graph

best performance among FGMs made of 2D materials. Our findings open new possibilities toward next generation nanoelectronics, such as artificial neuron network based on anisotropic memory arrays.

Results

Characterizations of ultra-thin GaTe. Bulk GaTe single crystals were prepared via flux method and were confirmed via x-ray diffraction (see Supplementary Fig. 1). We mechanically exfoliated the bulk and deposited ultra-thin GaTe flakes onto 285 nm silicon oxide grown on heavily doped silicon wafers for optical and electrical characterizations. It is known that GaTe has a layered structure with lattice symmetry of group C_{2h} (Fig. 1a), similar to that of 1T'-MoTe₂. The unit cell for a single layer GaTe is indicated in Fig. 1b. Monoclinic GaTe crystal is of very low symmetry, providing an ideal platform to study anisotropy¹². It is also known as a typical p-type semiconductor with a direct band gap of ~ 1.65 eV^{13,14}, which has many potential applications, such as photodetectors¹⁵, radiation detectors¹⁶, as well as thermophotovoltaic devices¹⁷. However, GaTe in air was reported to be easily oxidized¹⁸, leading to band gap restructuring in air, at the same time, the photoluminescence (PL) signal decreases and extra Raman peaks associated to oxides become more pronounced. Atomic Force Microscope (AFM) scan of a typical GaTe flake (14 nm in thickness) is shown in Fig. 1c, d. First, we characterized electronic transport of those flakes in air (Supplementary Figs. 2–6). However, without protection from air, the source-drain currents I_{ds} of devices made by GaTe flakes are rather low, with maximum current of a few nano amperes, in agreement with other reported results¹⁹. It is found that, without thermal annealing, few-layered GaTe devices are barely conducting, as shown in Supplementary Fig. 2. In the following, we will focus on the devices made by ultra-thin GaTe flakes encapsulated by hexagonal boron nitride (h-BN) in a glove box, in order to diminish damages from air. Detailed analysis of the effect of h-BN protection can be found in Supplementary Figs. 7–11.

Polarized Raman can be used to determine crystal orientation in 2D flakes^{10,12}, and also to deliver information of phonon modes that are related to the lattice symmetry. Supplementary Fig. 12 shows Raman spectra of a typical GaTe flake, with the angle-dependent intensity at Raman shift of 271.1 cm⁻¹ plotted in a polar figure overlaid on the optical image shown in the inset. A twofold symmetry of the polar figure can be seen, with one of the polarized axis parallel to the exfoliated straight edge of the GaTe itself. Such a Raman-active mode is a A_g mode in C_{2h} point group. From Raman tensor analysis, the direction of maximal Raman intensity of such A_g mode corresponds to the lattice direction with short lattice constant, defined as y direction in Fig. 1a, with x direction perpendicular to it. Raman mode at 164.6 cm⁻¹ is another good reference for determining the crystalline direction (see Supplementary Fig. 13)¹². Such a mode has a fourfold symmetry (B_g mode) and therefore four-lobe angular dependence, with each lobe 45 degrees away from the polarization axis of the mode at 271.1 cm⁻¹. By comparing Raman anisotropy with the anisotropy of electrical conductivity (shown in the next section), it is known that y axis of GaTe layer corresponds to a maximum conductivity (Supplementary Figs. 12–13). By this means, one can pattern electrodes for electrical measurements just with the zero angle defined along with such straight edges (y direction).

As shown in Fig. 1e, nine pairs of electrodes (20° angle between each two electrodes) were deposited onto the h-BN/GaTe/h-BN stack sample S1 (see Methods), which is further patterned into a circular shape in Fig. 1f. As a result, the source-drain current

I_{ds} along each pair of electrodes at gate voltage $V_g = -80$ V follows an ellipsoidal dependence of the testing angle, shown in Fig. 1g. It is rather straight forward that the maximum I_{ds} flows in 0° , which is parallel to one of the straight edges, i.e., the y axis, as marked in Fig. 1f. Such twofold ellipsoidal oscillation of in-plane anisotropic conductivity is also seen in a number of other 2D materials^{4,5,9–11,20}.

To unveil the origin of in-plane electrical conductivity anisotropy found in ultra-thin GaTe, we performed first-principles electronic structure and non-equilibrium Green's functional quantum transport calculations with a simplified model on GaTe monolayer. Electronic band structure along high-symmetry lines is shown in Fig. 1h, with the first Brillouin zone and high-symmetry points defined in Fig. 1i. A direct band gap of 1.5 eV locates at the X point, in agreement with PL measurement in Supplementary Fig. 14. Thanks to the direct band gap, outstanding photo responses have been reported in GaTe devices^{15,21}. What's very interesting is the strongly anisotropic band dispersion obviously seen along two perpendicular directions (Γ - X and X - K). At the VBM, band dispersion along Γ - X is much bigger than along X - K , which gives rise to strong anisotropic effective mass m^* at VBM, as shown in Supplementary Fig. 15. The calculated m^* (shown in Supplementary Fig. 16) along X - K direction is ~ 10 times larger than that along Γ - X , which seems to lead to a better transport property along x axis than y axis. However, deformation potential E_1 (shown in Supplementary Fig. 16) due to electron-phonon scattering shows an opposite trend to m^* in both x and y axes, and dominates over the anisotropy of effective mass to give rise to the anisotropy of electrical conductivity σ according to the deformation potential theory (see Methods), σ_y is about five times as big as σ_x at low doping. When plotting experimental data in the renormalized conductivity polar figure in Fig. 1j, a twofold symmetry of conductance can be clearly seen.

Gate-tunable GAR in ultra-thin GaTe. The above-mentioned twofold in-plane symmetry of resistivity can be reproduced in multiple GaTe devices (Supplementary Figs. 17–18), and we performed a systematic study on the sample S2. As shown in Fig. 2a, with the same GaTe flake (optical image of the device is shown in the inset of Fig. 2a), field-effect curves, measured at source-drain voltage $V_{ds} = 2$ V along x and y directions, exhibit strong anisotropy, indicated by red and blue colors, respectively. I_{ds} measured along the 12 directions with a fixed $V_{ds} = 5$ V are plotted at $V_g = -60$ V, while an ellipsoidal oscillation at all angles with 2π periodicity can be seen, shown in Fig. 2b. When the gate voltages were swept from -60 V to -30 V, the maximum-to-minimum I_{ds} ratio of the ellipsoidal oscillation at each gate voltage varies largely. Note that similar gate-tunable anisotropic resistance behavior is also seen in bare GaTe devices without BN encapsulation (Supplementary Figs. 19–20).

Taking y (0°) and x (90°) directions for examples, closer look of I - V output curves in the range of ± 5 V is shown in Fig. 2c–d. It is seen that at high bias voltage, I_{ds} for direction y is varying within 10^{-7} and 10^{-5} A, whereas I_{ds} for direction x is varying within 10^{-11} and 10^{-6} A. We define the electrical maximum anisotropic ratio Γ_a as I_y/I_x for each fixed gate voltage. Strikingly, as extracted from Fig. 2b, Γ_a as a function of gate voltage shows a gate-tunability from less than one order to as large as 10^3 . This gate-tunable GAR effect was not found in previous studies. We fabricated various samples in similar configuration of h-BN encapsulated ultra-thin GaTe devices (Supplementary Figs. 21–23), with their Γ_a plotted together in Fig. 2e. In general, anisotropic ratio in those devices can be gate tuned from a few times, to several hundreds or even thousands folds, which is much higher than other 2D systems

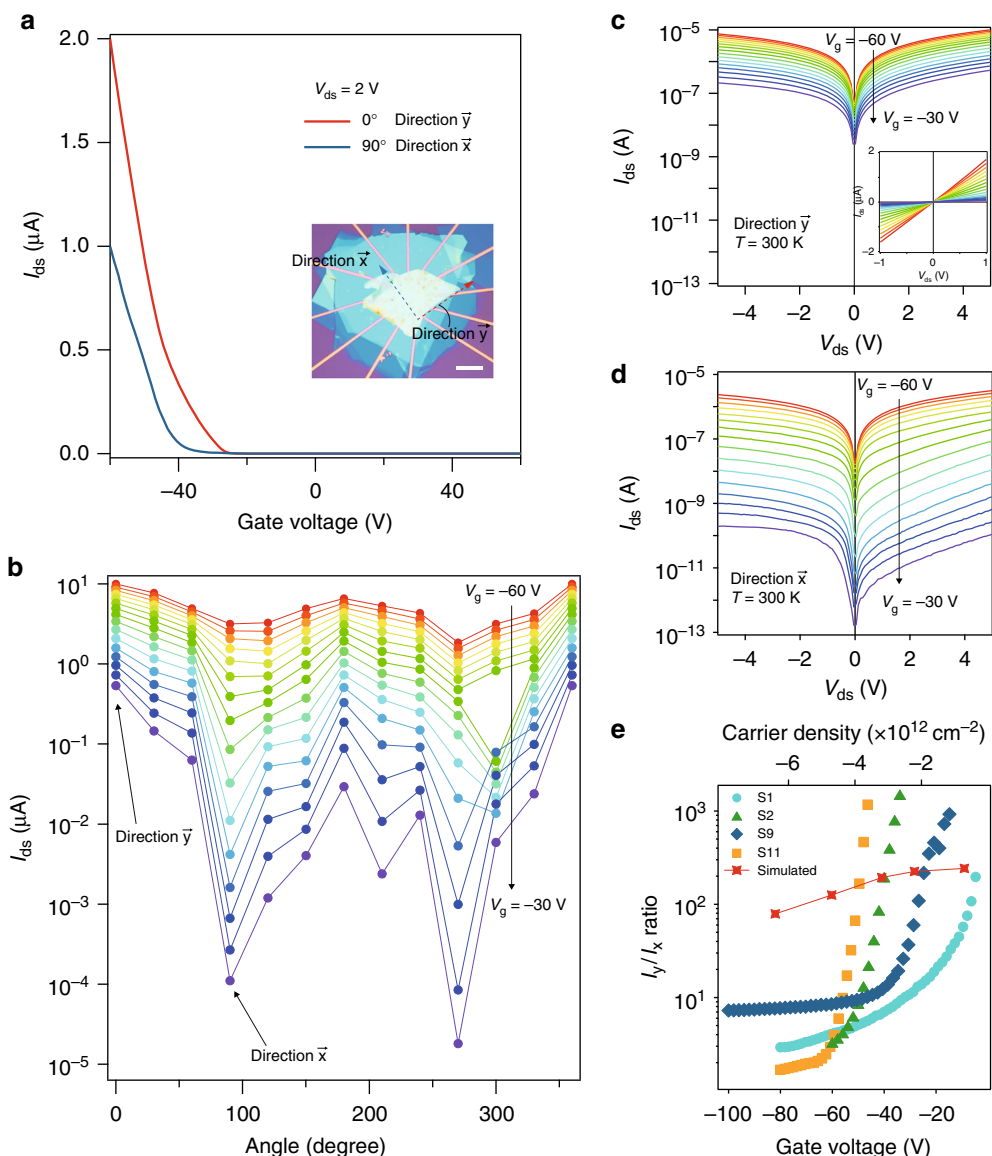


Fig. 2 Giant anisotropic resistance in ultra-thin GaTe. **a** Field effect curves of a typical GaTe device (Sample S2) recorded along x and y directions, with the optical image of the device shown in the inset. Scale bar in the inset is $10\ \mu\text{m}$. **b** I_{ds} of the same device measured along the 12 directions with a fixed $V_{\text{ds}} = 5\ \text{V}$, and with the gate voltages swept from $-60\ \text{V}$ to $-30\ \text{V}$. **c**, **d** I - V curves plotted in log scale at $V_{\text{ds}} = \pm 5\ \text{V}$ of the same device measured along y and x directions, respectively. The gate voltages were swept from $-60\ \text{V}$ to $-30\ \text{V}$. Inset of **c** shows the corresponding data in linear scale. **e** The maximal electrical anisotropic ratio $I_{\text{y}}/I_{\text{x}}$ extracted from different samples (denoted as S1, S2, S9, and S11) as a function of gate voltage

reported so far^{4,5,7,9,22}. To push the 2D limit of the GaTe thicknesses studied in this work, we managed to fabricate sample of GaTe with $\sim 4.8\ \text{nm}$ in thickness. And as the inter-layer distance of GaTe is $\sim 0.8\ \text{nm}$ ²¹, we can draw the conclusion that, down to the six-layer limit, the observed GAR prevails, as shown in Supplementary Fig. 24.

As I_{a} in ultra-thin GaTe is rather weak at relatively higher hole doping (say, in the $V_{\text{g}} = -60\ \text{V}$ limit), and becomes significantly enhanced close to the VBM in the vicinity of $V_{\text{g}} = -30\ \text{V}$, it more or less shows a better electron collimation at higher I_{a} values, i.e., electrons tend to flow preferably along a certain direction at those conditions. Considering the deformation potential theory only applied to the band edge (VBM or CBM) and its inability to take care the gate-tunability on electronic transport^{23,24}, we calculate I - V curves and their gate dependence by combining density functional theory (DFT) calculation with the non-equilibrium Green's function (NEGF) method²⁵ (see Methods),

and show calculated field effect I - V data at $V_{\text{ds}} = 0.5\ \text{V}$ along two perpendicular crystalline directions in Supplementary Fig. 25. To avoid possible contact Schottky barrier, we use p -type heavily doped GaTe as source and drain. I - V curves along both x and y directions show a similar behavior to the experimental ones as given in Fig. 2a. $I_{\text{y,ds}}$ at $V_{\text{ds}} = 0.5\ \text{V}$ increases from $1.39\ \mu\text{A}$ at $V_{\text{g}} = -9.1\ \text{V}$ to $12.52\ \mu\text{A}$ at $V_{\text{g}} = -82\ \text{V}$. More strikingly is the gate dependence of $I_{\text{x,ds}}$, which changes by two orders of magnitude, from $4.63 \times 10^{-3}\ \mu\text{A}$ at $V_{\text{g}} = -9.1\ \text{V}$ to $0.19\ \mu\text{A}$ at $V_{\text{g}} = -82\ \text{V}$. The calculated $I_{\text{y}}/I_{\text{x}}$ ratio, given in filled red squares in Fig. 2e, decreases with increasing gate voltage, from ≈ 300 at $-9.1\ \text{V}$ to ≈ 60 at $-82\ \text{V}$, agreeing qualitatively with the experimental ratio but in a milder way than the experimental data. The discrepancy can be ascribed to that extrinsic effect in experiment such as nonlinear contact resistivity is not taken into account in the simulated device. Nevertheless, the gate-tunable GAR can still be intrinsically analyzed from the calculated

transmission coefficient, as shown in Supplementary Fig. 26. At low gate voltage (-9.1 V), there is almost no x direction transmission channels in the scattering region between source energy level E_L and drain energy level E_R , whereas a sizeable y direction transmission is observed, giving rise to a large anisotropic ratio Γ_a at low gate voltages. In contrast, at high gate voltage (-82 V), non-zero transmission coefficient in channel material appears with comparable total transmission in both x and y directions, greatly suppressing GAR in GaTe.

Ultra-thin GaTe anisotropic floating gate memory. It is of great importance to demonstrate conceptual devices taking advantage of the GAR effect in ultra-thin GaTe. In the following, we will discuss a prototype anisotropic memory based on ultra-thin GaTe. Using the vdW assembly method (see Methods), a few-layered graphene was equipped in addition to the h-BN/GaTe/h-BN sandwich, forming an architecture of FGM. Optical image and art view of such typical devices are shown in Fig. 3a, b.

Interestingly, when sweeping within the same gate window, the hysteresis memory curves along y and x directions vary largely, with a clear discrepancy of memory window size, shown in Fig. 3c, d. This result is more pronounced in a log scale when plotted together in Fig. 3e. One can see that after an operation of erasing (sweep the V_g from 0 V to -20 V , and back to 0 V), the device stays in an “Off” state in both directions. While an program operation (sweep the V_g from 0 V to 20 V , and back to 0 V), the device stays in two different “On” states in y and x directions, as indicated by colored circles in Fig. 3e, and their corresponding retention in Fig. 3f. It thus makes the device an anisotropic memory, i.e., one single operation of programming-erasing will generate two sets of data in the two directions, making the device conceptually compatible with direction-sensitive data storage.

Discussion

To verify the performance of ultra-thin GaTe FGM with graphite floating gate along fixed direction, we recorded polarization

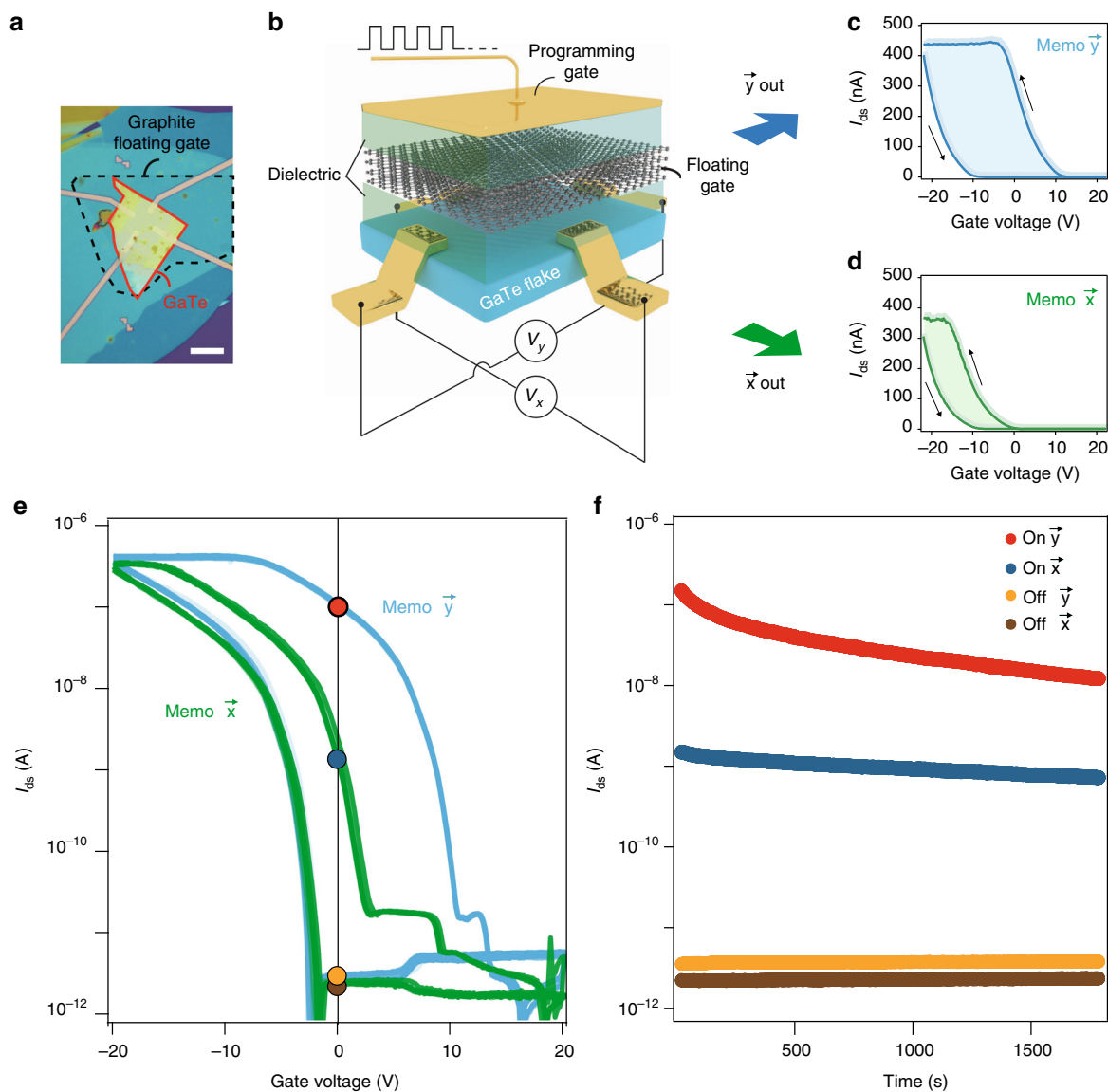


Fig. 3 Anisotropic ultra-thin GaTe floating gate memory. **a, b** Optical image and art view of a typical h-BN/GaTe/h-BN device (Sample S6) with a graphite floating gate. Scale bar in **a** is $10\ \mu\text{m}$. **c, d** Memory curves measured along x and y directions, respectively. **e** Same data in **c** and **d**, plotted in log scales, with 10 repeated measurements (indicated by changing the gradient of the green and blue colors). **f** Retention time of memory at $V_g = 0\text{ V}$, along y and x directions, with on and off positions indicated by the colored circles in **e**. $V_{ds} = 2\text{ V}$ was used in the above measurements

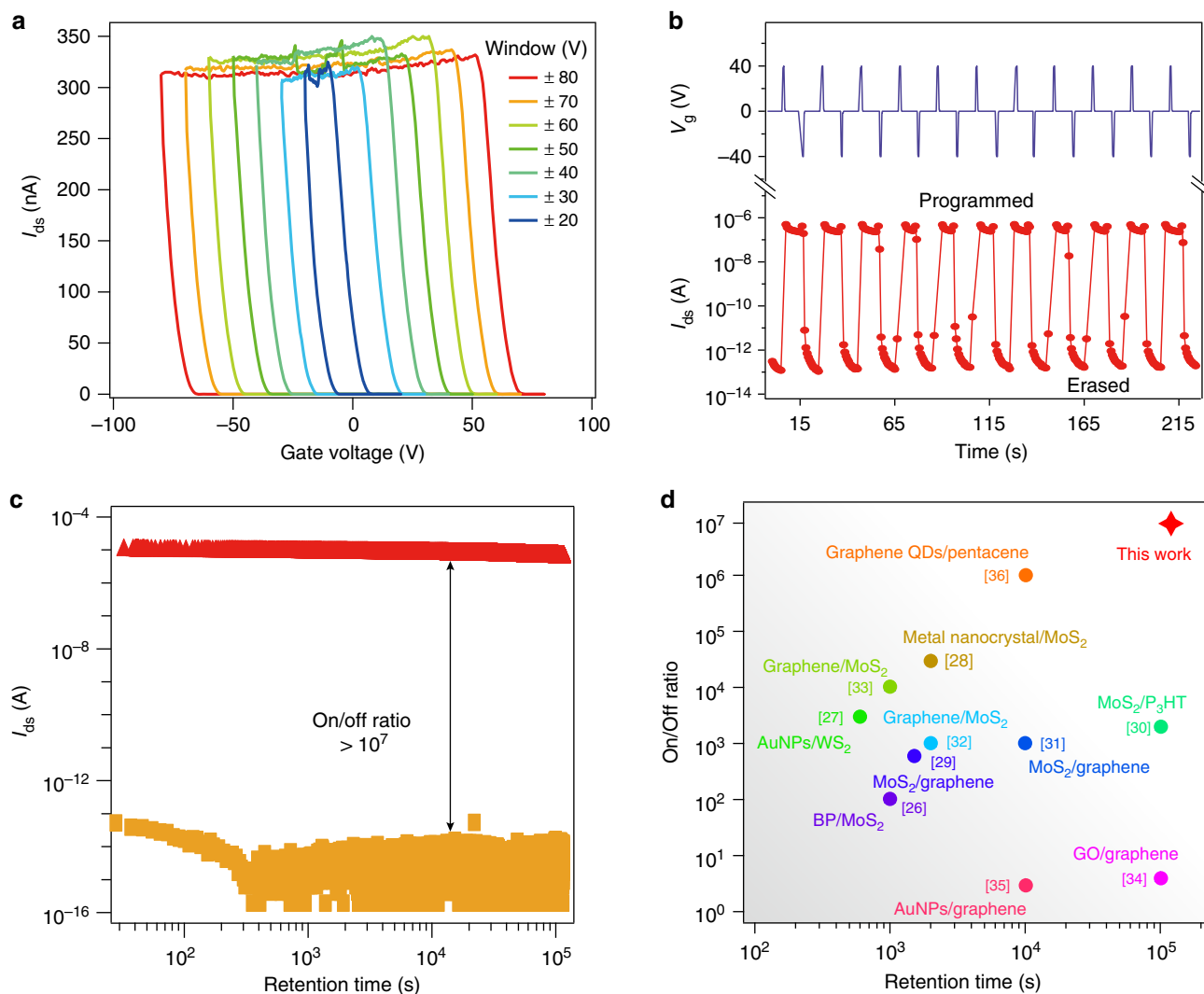


Fig. 4 Comparison of the floating gate memory performance of GaTe with other 2D materials. **a** Memory windows measured in y direction. **b** Demonstration of erasing and programming pulses measured in y direction. **c** Retention time test of the device at on and off states. **d** Summary of the performance of FGM made by 2D materials. Data in **a**, **b** are measured in sample S6, and data in **c**, **d** are measured in sample S4. $V_{ds} = 2$ V was used in the above measurements

gate voltages for different ranges from ± 20 V to ± 80 V in direction y , shown in Fig. 4a (see also Supplementary Figs. 27–28). It can be seen that the GaTe memory shows rather stable erased state in all gate ranges. Once fed with the stimulation of pulsed V_g of ± 40 V, the device can be readily erased and programmed as illustrated in Fig. 4b.

In the following, we compare the GaTe FGM with the state-of-the-art FGMs fabricated from other 2D materials^{26–36}. Given that retention of the erased and/or programmed states is one of the most important parameters of such FGM, we recorded along direction y the on state (by a positive gate pulse), and the off state (by a negative gate pulse), respectively. Among GaTe FGM devices tested, the best performance (measured from sample S4 as shown in Fig. 4c) exhibits an on/off ratio exceeding 10^7 and the attenuation of the on/off ratio is $< 5\%$ in a retention time of 10^5 s (detailed memory characterizations of sample S4 are shown in Supplementary Fig. 29). By summarizing the state-of-the-art performance of FGM based on 2D materials, it is found that, our h-BN/GaTe/h-BN with graphite floating gate memory shows up to now the record on/off ratio and retention time, as shown in Fig. 4d. We attribute the observed high on/off ratio in the h-BN encapsulated devices to the better preserved band gap in

the pristine GaTe. When the Fermi level is tuned to be inside the band gap (no electron density of state available), the off-state current is at the order of pA, whereas the on-state current reaches a few μ A. To illustrate the working principle of the GaTe floating gate memory devices, we show, according to previous studies^{26,27,29,33}, simplified band diagram in Supplementary Fig. 30.

In conclusion, we have discovered that ultra-thin GaTe encapsulated by h-BN devices show a twofold symmetry electrical conductance oscillations along different in-plane directions, with their maximum anisotropic ratios I_y/I_x gate-tunable in the range from < 10 to a few thousands. This GAR arises from the in-plane anisotropic transmission coefficients, and the anisotropic ratio can be changed by several orders of magnitude mainly owing to the sensitivity of x direction conduction channel to gating. Based on this GAR effect, we devised an anisotropic GaTe memory with a vdW assembled graphite floating gate. The prototype memory devices show direction-sensitive multiple-level output non-volatile memory behavior when measured from different directions. Moreover, fixed direction measurements suggest that the GaTe FGMs show record performances in terms of both on/off ratio and retention time among the state-of-the-art FGM based

on 2D materials. Using this unit cell of GaTe anisotropic field effect transistor as a building block, it can be further expanded into many possible applications such as neural computation with GaTe FGM neural network arrays.

Methods

Single crystal GaTe was prepared via the self-flux method. Raw bulk materials with stoichiometric ratio of Ga (purity 99.999%): Te (purity 99.9%) = 48.67:51.33 were mixed and kept at 880 °C for 5 h. The mixture was then cooled at the rate of 1.5 °C h⁻¹, followed by a natural cooling process. The h-BN (crystals from HQ Graphene) encapsulated GaTe devices were fabricated using the dry-transfer methods (Supplementary Fig. 31)³⁷, and then annealed in Ar:H₂ (10:1) mixture at 320 °C for 30 mins before electrical measurements.

The h-BN-encapsulated GaTe heterostructures were fabricated in an mBraun-universe glove box. A Bruker Dimension Icon AFM was used for thicknesses and morphology tests. Raman measurements were performed by an HR 800 JobinYvon Horiba polarized Raman spectroscopy. The electrical performances of the devices were measured using a semiconductor analyzer (Agilent B1500A) and a probe station (Cascade Microtech Inc. EPS150) under ambient conditions.

The electronic band structure in this work was calculated by using the first-principles density functional theory as implemented in the VASP code³⁸. Projector augmented wave pseudopotentials³⁹ and the Perdew-Burke-Ernzerhof⁴⁰ functional were, respectively, used to describe electron-ion interaction and electronic exchange-correlation interaction. We adopted 500 eV as the electronic kinetic energy cutoff for the plane-wave basis and 10⁻⁶ eV as the criterion for reaching self-consistency. The Brillouin zone (BZ) of the primitive unit cell (12 atoms per cell) was sampled by 20 × 20 × 1 k-points⁴¹. Rectangle supercell (24 atoms per cell) was used to calculate anisotropic electrical conductivity and the BZ was sampled by 2 × 6 × 1 k-points.

The electrical conductivity σ was evaluated based on $\sigma = ne\mu$, in which carrier mobility μ was calculated based upon the deformation potential theory with formula^{23,24}

$$\mu = \frac{e\hbar^3 C_{2D}}{k_B T m^* m_d E_1^2}, \quad (1)$$

where \hbar is the reduced Planck constant, C_{2D} is the elastic modulus derived from $(E - E_0)/A_0 = C\varepsilon^2/2$ (E , E_0 , A_0 , C , and ε denote, respectively, the total energy, the total energy at equilibrium, the area of the 2D unit cell at equilibrium, elastic constant, and the lattice strain), k_B is the Boltzmann constant, T is temperature, m^* is the effective mass in the transport direction, m_d is the averaged effective mass defined by $m_d = \sqrt{m_x^* m_y^*}$, and E_1 is the deformation potential constant of the VBM along the transport direction. E_1 defined by $E_1 = \Delta V/\varepsilon$ with ΔV as the energy change of the VBM under small strain ε .

I - V curve of the GaTe transistor was simulated using the DFT coupled with the NEGF method²⁵, as implemented in the ATK package⁴². The structure of GaTe transistor is shown in Supplementary Fig. 25(a). We employed the Dirichlet boundary condition to ensure the charge neutrality in the source and the drain region. The temperature was set to 300 K. The density mesh cutoff was set to 80 Hartrees. The Monkhorst-Pack k-point meshes for device along the x and y direction were sampled with $40 \times 6 \times 1$ and $114 \times 6 \times 1$, respectively. Electron-ion interaction was treated by SG15 Optimized Norm-Conserving Vanderbilt (ONCV) pseudopotentials^{43,44}. The transmission coefficient at energy E was averaged over 31 k-points perpendicular to the transport direction. The generalized gradient approximation was adopted for the electronic exchange-correction functional. The length of scattering region is 9.530 nm and 9.676 nm for transistor along x and y directions, respectively, both of which are sufficiently large to avoid interaction between source and drain. The code of VASP (www.vasp.at) and QuantumATK (<https://docs.quantumwise.com/guides/guides.html>) are commercially available from their official websites.

Data availability

The data that support the findings of this study are available from the corresponding authors upon reasonable request.

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Author contributions

Z.H., Z.Z. and T.Y. conceived the experiment and supervised the overall project. H.W., X.S., J.C. fabricated the devices. H.W., M.C., X.S., X.L., Y.Y. and Z.H. carried out electronic transport measurements; M.Z., C.Q., X.Z., L.X., J.Z., S.C. and J.C. carried out optical measurements; Y.W., B.D. and T.Y. conducted the theoretical simulations. J.H.

and H.G. did the simulations on polarized Raman. D.S. contributed in sample fabrications. L.Z. and W.L. grew the GaTe bulk crystals. K.S., J.W. and Y.H. carried out TEM performances. The manuscript was written by Z.H., T.Y. and H.W. with discussion and inputs from all authors.

Additional information

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