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Reliable Nonvolatile Memory Black Phosphorus Ferroelectric Field-Effect Transistors with van der Waals Buffer

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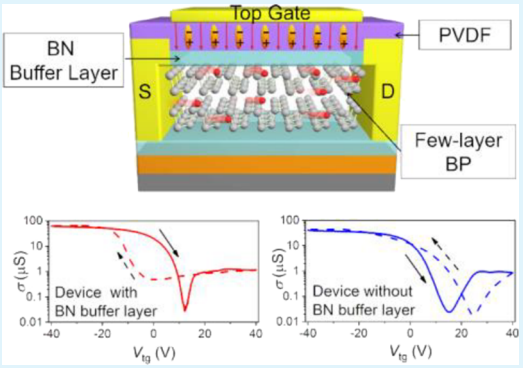
Supporting Information

ABSTRACT: Two-dimensional material-based ferroelectric field-effect transistors (2D-FeFETs) hold great promise in information storage and processing. However, an often-observed and hard-to-control anti-hysteresis response of 2D-FeFETs, for example, hysteretic switching of the resistance states of the devices opposite to that of the actual polarization of the ferroelectric dielectric, represents a major issue in the industrial applications of such devices. Here, we demonstrate a van der Waals buffer technique that eliminates anti-hysteresis in black phosphorus (BP) 2D-FeFETs and restores their intrinsic hysteretic behavior. Our modified BP 2D-FeFETs showed outstanding performance including high room-temperature carrier mobility, robust bistable states with fast response to a gate, a large on/off ratio at zero gate voltage, a large and considerably more stable memory window, and a long retention time. During repeated gate operation, the memory window of the buffered device is ∼7000 times more stable than the unbuffered device. Such a method could be crucial in future information technological applications that utilize the intrinsic properties of 2D-FeFETs.



KEYWORDS: *black phosphorus, P(VDF-TrFE), nonvolatile ferroelectric memories, field-effect transistors (FETs), anti-hysteresis*

INTRODUCTION

Since the discovery of graphene, two-dimensional (2D) van der Waals materials have attracted significant attention for their unique optical, electrical, mechanical, and thermal properties.[1−8] Black phosphorus (BP), known as phosphorene when thinned down to a single layer, is a 2D semiconductor with a puckered honeycomb structure.[9] Few-layer BP (FLBP) is considered a highly promising candidate for nanoelectronics and optoelectronics applications due to the simultaneous presence of a high on/off ratio, high mobility, and direct band gap in the materials.[10−16]

Recently, a surge of interest has been seen in the research of heterostructures of 2D materials and ferroelectric materials for the development of two-dimensional material-based ferroelectric field-effect transistors (2D-FeFETs), which have potential benefits in terms of reduced power consumption, alleviated short channel effects, and faster switching.[17−27] Similar to their 3D counterparts, the principles of operation for 2D-FeFETs is the controlled switching of the resistance states (defined as the ON and OFF states) due to the ferroelectric switching of the polarization of the dipole moments in the ferroelectric materials, usually tuned by a large enough coercive gate voltage. For an intrinsic 2D-FeFET, a pronounced hysteresis behavior in the resistance should be observed, which matches the hysteretic behavior in the electrical dipole moment of the ferroelectric layer. However, many studies in 2D-FeFETs show inverse hysteretic behavior in the switching of the resistance states (we shall call it "anti-hysteresis" behavior throughout this paper).[26−30] Besides, the memory window V_{Mem} of anti-hysteretic 2D-FeFETs usually varies with

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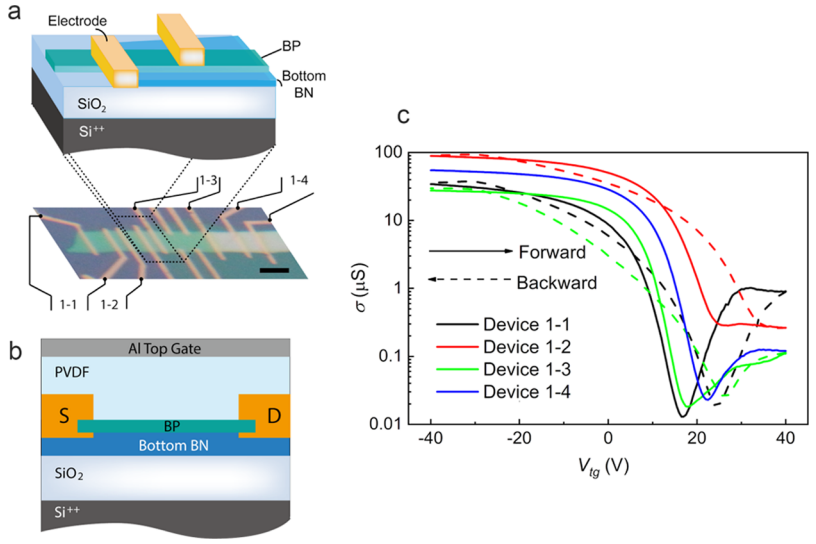

Figure 1. Device structure and anti-hysteretic $\sigma(V_{tg})$ behavior. (a) Structural information for devices 1-1 to 1-4. Schematic view of devices 1-3 and 1-4 before spin-coating of the P(VDF-TrFE) film (upper panel) and optical image of the devices (lower panel). The scale in the optical image is 5 μm. (b) Schematic side view of devices 1-3 and 1-4 after deposition of the top gate. (c) Anti-hysteretic behavior in $\sigma(V_{tg})$ for devices 1-1 to 1-4 with V_{tg_max} = 40 V.

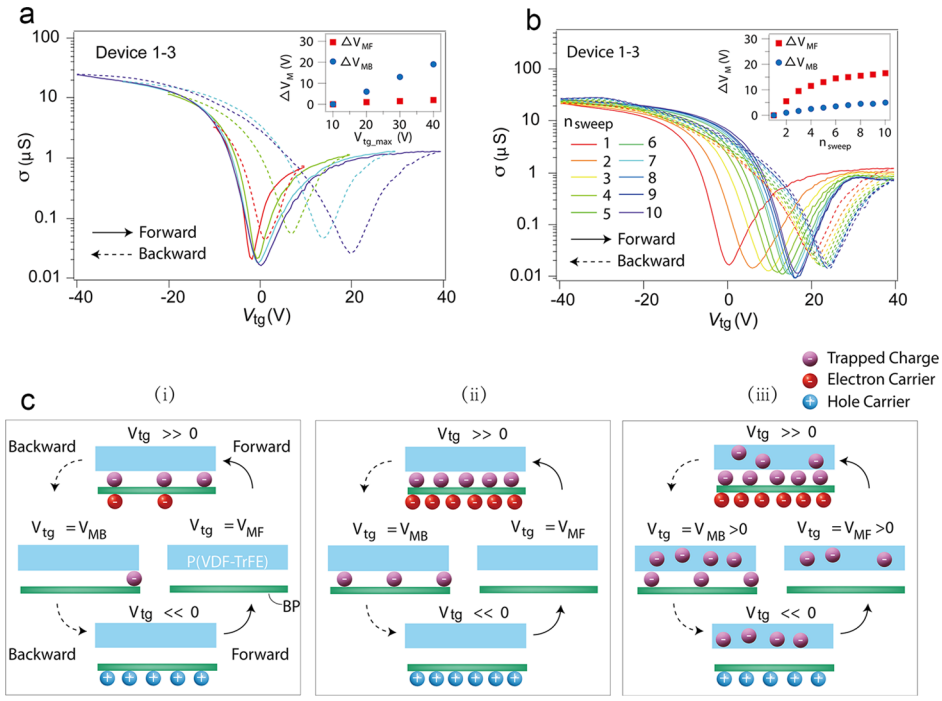

Figure 2. Dynamic response of the anti-hysteretic $\sigma(V_{tg})$ behavior. (a) $\sigma(V_{tg})$ curves measured with increasing V_{tg_max} (from 10 to 40 V, in steps of 10 V). Inset shows V_{MF} and V_{MB} versus V_{tg_max}. (b) $\sigma(V_{tg})$ curves measured repeatedly at a fixed V_{tg_max} of 40 V. Inset shows V_{MF} and V_{MB} versus n_{sweep}. (c) Schematics for the physical process of trapping and detrapping of electrons in the BP-P(VDF-TrFE) device: (i) with small V_{tg_max}, (ii) with large V_{tg_max}, and (iii) after charging the PVDF thin film several times with large V_{tg_max}.

the gate sweeping range and varies with time (see the definition of the memory window in Methods). It is generally believed that the overall gate voltage cycling performance of 2D-FeFETs is a result of the competition between the interfacial charging (extrinsic effects) and the dipole moments exerted by the ferroelectric layer (intrinsic effects). However, the exact nature of the interface charge traps that is responsible for the anti-hysteresis behavior is still in dispute from surface absorbates at the channel/dielectric interface[27−29] to the charge traps present in the ferroelectric materials.[29−31] Remarkably, a few studies have been carried out on improving the interface conditions and to control the hysteresis direction in 2D-FeFETs.[27,31,32] The uncertainty of the hysteresis direction and its magnitude has been a significant obstacle for technological applications of ferroelectric-gated devices.

EXPERIMENTAL SECTION

In this work, we investigated nonvolatile devices based on FLBP using poly(vinylidenefluoride-*co*-trifluoroethylene) [P(VDF-TrFE)] as the ferroelectric gate dielectric. We demonstrate that the injection of

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electrons (instead of holes) from the BP channel into the charge traps of P(VDF-TrFE) is the origin of the anti-hysteresis in devices with conventional structures. Furthermore, we develop a van der Waals buffer technique to eliminate the parasitic effects from the charge traps in the P(VDF-TrFE) layer. Our modified BP-P(VDF-TrFE) nonvolatile devices showed outstanding performance including high room-temperature carrier mobility, robust bistable states with fast response to a gate, large on/off ratio at zero gate voltage, a large and considerably more stable memory window, and a long retention time. The experiment shows that the van der Waals buffer technique works well in restoring the intrinsic switching characteristics of BP-P(VDF-TrFE), and the modified BP-P(VDF-TrFE) devices are a strong candidate for future nonvolatile memory devices based on 2D materials.

Anti-Hysteresis in Unbuffered BP-P(VDF-TrFE) 2D-FeFETs. Unbuffered BP-P(VDF-TrFE) 2D-FeFETs, where BP has a direct interface with the P(VDF-TrFE) ferroelectric layer, were fabricated as controlled devices. Such unbuffered devices consist of FLBP as the conduction channel, a ferroelectric top gate, and an ordinary (nonferroelectric) back gate (see details in Methods). Four such devices were made from a single piece of FLBP crystal on a hexagonal boron nitride (BN) substrate or on a SiO_2 substrate, named devices 1-1, 1-2, 1-3, and 1-4. The schematic and optical images of the unbuffered BP 2D-FeFETs are shown in Figure 1a. The schematic side view of the devices after deposition of the top gate is shown in Figure 1b. The thickness of the BP flake was measured by atomic force microscopy (AFM) to be 15 nm for devices 1-1, 1-2, and 1-3, and 25 nm for device 1-4 (see Supporting Information, Figure S1). Figure 1c depicts the conductivity versus top gate voltage curves ($\sigma(V_{tg})$) of devices 1-1 to 1-4 when sweeping V_{tg} in a closed loop (from −40 to 40 V and then from 40 to −40 V). The ferroelectric polarization curve of the P(VDF-TrFE) thin film is provided in Supporting Information, Figure S2. The different line styles in Figure 1c indicate different gate sweeping directions, with the solid lines for V_{tg} sweeping from negative to positive values (forward sweeps) and the dashed lines for the opposite sweeping direction (backward sweeps). Such line styles will be used throughout this paper. In order to avoid unwanted charge accumulations, when we sweep V_{tg}, V_{bg} is set to zero, and V_{tg} is set to zero when we sweep V_{bg} throughout this experiment. As can be seen in Figure 1c, all the unbuffered devices exhibit anti-hysteresis behavior regardless of whether the bottom surface of BP is in contact with BN or SiO_2. This is consistent with the competing effects of interface charging and the polarization of the P(VDF-TrFE) layer in these devices. The hysteretic reversal of the electric polarization in the P(VDF-TrFE) layer will cause the normal hysteresis behavior in $\sigma(V_{tg})$; the charge trapping−detrapping process, however, will cause anti-hysteresis behavior in $\sigma(V_{tg})$.[33−35] Hence, when the density of the charge traps is large enough, the effect of trapped charges injected from BP dominates, which results in an anti-hysteretic behavior. Such a mechanism naturally leads to an uncertain magnitude of the anti-hysteretic behavior (depending on the number of populated charge traps) and a relatively slow switching process (as compared to the reversal of the electric dipole moment of the ferroelectric layer[26,36]).

Nature of Charge Traps. In order to determine the nature of the charge traps and the trap charging dynamics in the P(VDF-TrFE) layer, we investigated the dynamic response of the hysteretic behavior on the sweep range (Figure 2a) and on the number of repeated sweeps at a fixed sweep range (Figure 2b). Here, we define the sweep range as V_{tg_max}, which means that we cycle V_{tg} in a close loop between $-V_{tg\_max}$ and V_{tg_max}. As can be seen from Figure 2a, the anti-hysteretic behavior becomes more pronounced with increasing the gate sweep range (from ±10 to ±40 V, in steps of 10 V). Furthermore, the top gate voltage at the minimum conductivity (V_M) shows systematic changes with an increasing gate sweep range. Here, we define the change of V_M as $\Delta V_M = V_M(n\text{th sweep}) - V_M(1\text{st sweep})$ and define ΔV_M of forward and backward sweeps as ΔV_{MF} and ΔV_{MB}, respectively. As shown in the inset of Figure 2a, with an increasing gate sweep range, both ΔV_{MF} and ΔV_{MB} increase with distinctive asymmetry: ΔV_{MB} has pronounced and positive dependence on the sweep range (e.g., $\Delta V_{MB}(V_{tg\_max}) > 0$), while the dependence of ΔV_{MF} on V_{tg_max} is also positive (e.g., $\Delta V_{MF}(V_{tg\_max}) > 0$) but much weaker ($\Delta V_{MB} \gg \Delta V_{MF}$).

To understand such behavior, we look into three possible sources that can cause a nonzero ΔV_M, namely, ferroelectric polarization, interface absorbate-associated charge trapping, and material-specific charge traps. For a ferroelectric layer that is undergoing initial polarization, an increase in V_{tg_max} could indeed cause more polarization in the thin film and thus a nonzero ΔV_M, only if $V_{tg\_max} < V_c$. Here, V_c is the coercive voltage to completely polarize the ferroelectric thin film. Since V_c for our 300 nm P(VDF-TrFE) layer is about 22.5 V (ref 18), for $V_{tg\_max} > 22.5$ V (as shown in the inset of Figure 2a), we should see no contribution of progressive dipole alignment to ΔV_M,(e.g., ΔV_M should be zero for $V_{tg\_max} > V_c$). Furthermore, for $V_{tg\_max} < V_c$, we should have $\Delta V_{MB} < 0$ and $\Delta V_{MF} > 0$ in this case (in the case of normal hysteresis), which is again different from the experimental data. Thus, the nonzero ΔV_M is not from ferroelectric polarization.

For anti-hysteresis caused by the interface absorbate-associated charge trapping, V_M is supposed to respond symmetrically for forward and backward sweeps;[26,29] for example, we should see that $\Delta V_{MB} > 0$, $\Delta V_{MF} < 0$, and $|\Delta V_{MF}| \approx |\Delta V_{MB}|$, contrary to experimental observation. Thus, the nonzero ΔV_M is not from the interface absorbate-associated charge trapping either.

Based on the above reasons, the experimentally observed positive and asymmetric ΔV_{MB} and ΔV_{MF} in our unbuffered BP-P(VDF-TrFE) 2D-FeFETs indicate that the source of anti-hysteresis is the material-specific electron traps (traps that can only be neutral or be negatively charged).[37,38] In such a picture, ΔV_{MB} should be a function of V_{tg_max}, and ΔV_{MF} should be independent of V_{tg_max} and be close to zero when trapped charge diffusion can be neglected. Indeed, that is what is experimentally observed. The difference in gate voltage of minimum conductance between backward sweeping and forward sweeping in one sweep loop, $\Delta V_{min} = V_{MB} - V_{MF}$, can be used to estimate the effective trap density $N_{trap} = C_g \Delta V_{min}/2e$ where C_g is the gate capacitance and e is the elementary charge. From Figure 2a, we extract a linear relation between ΔV_{min} and V_{tg_max}: $\Delta V_{min} = 0.55 \times V_{tg\_max} - 2.75$. The trap density can also be calculated as $N_{trap} = -\int_{E_0}^{E_F} D_{trap}(E)dE$ where $D_{trap}(E)$ is the energy-dependent trap density, E_0 is the charge neutrality energy, and E_F is the Fermi energy controlled by V_{tg}. The linear relation between N_{trap} and V_{tg_max} implies that D_{trap} in P(VDF-TrFE) is a constant of energy level E, similar to the case of SiO_2.[39] The slight dependence of ΔV_{MF} on V_{tg_max} can be understood as a diffusion process explained in the following paragraph. Figure 2c(i),(ii) shows the schematic physical process of trapping and detrapping of electrons at the BP-P(VDF-TrFE) interface at small and large V_{tg_max} values, respectively.

After the initial V_{tg} sweeps with increasing V_{tg_max}, we fixed the sweep range at ±40 V and sweep V_{tg} repeatedly. The response of the device under such a repeated sweeping sequence is shown in Figure 2b. It can be seen that with a fixed V_{tg_max}, ΔV_{MB} and ΔV_{MF} are still positive with each sweep repetition (e.g., ΔV_{MB} (n_{sweep}) > 0 and ΔV_{MF} (n_{sweep}) > 0 where n_{sweep} is the number of repeated sweeps with V_{tg_max} = 40 V). Contrary to Figure 2a, we see much more changes in the forward sweep: ΔV_{MB} (n_{sweep}) ≪ ΔV_{MF} (n_{sweep}) (see the inset of Figure 2b). This is consistent with the picture where the electrons diffuse from the surface charge traps to deeper charge traps due to charge density gradient, as illustrated in Figure 2c(iii). Deeper trapped charges are harder to deplete with a negative gate voltage, and given the limited time for $V_{tg} \ll 0$ during a gate sweep, the total number of populated electron traps in the P(VDF-TrFE) layer increases with each sweep, resulting in a relatively large and positive ΔV_{MF} (n_{sweep}). On the other hand, ΔV_{MB} is largely determined by the accessible surface traps with a certain V_{tg_max} (see Figure 2a) and should show weaker dependence on n_{sweep}. All the above experimental evidence is converging to the ansatz that the charge traps instead of the surface absorbates are responsible for the V_{tg_max}-dependent and time-dependent anti-hysteresis observed in our unbuffered BP-P(VDF-TrFE) devices, and the charge traps are electron traps.

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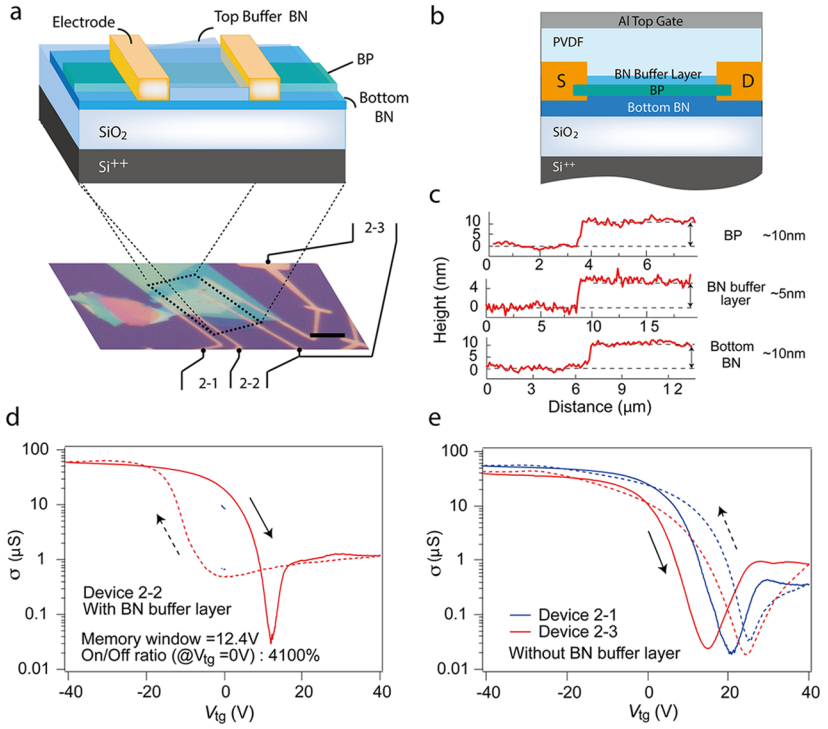

Figure 3. Device structure and $\sigma(V_{tg})$ curves for device 2. (a) Structural information of devices 2-1 to 2-3. Schematic view of device 2 before spin-coating of the P(VDF-TrFE) film (upper panel) and their optical image (lower panel). The scale in the optical image is 10 μm. (b) Schematic side view of the BP 2D-FeFET with the ultrathin BN buffer layer. (c) Thicknesses of the channel BP, BN buffer layer, and bottom BN determined by AFM. (d) Red lines: hysteretic $\sigma(V_{tg})$ loop of device 2-2; blue short lines: $\sigma(V_{tg})$ with a range of ±0.5 V after a 300 ms pulse of V_{tg} at −40 V (upper) or at +40 V (lower) to polarize the P(VDF-TrFE) polymer. (e) Anti-hysteresis $\sigma(V_{tg})$ loops of the unbuffered devices 2-1 and 2-3 from the same FLBP crystal.

Interface Engineering for BP-P(VDF-TrFE) 2D-FeFETs. Since the trapping−detrapping dynamics is relatively slow and produces an anti-hysteresis behavior varying in magnitude, it is highly desirable to minimize the effects of charge traps in future ferroelectric memory devices. We proposed a universal interface engineering technique to eliminate the anti-hysteresis behavior in 2D-FeFETs. The idea is to insert an ultrathin dielectric buffer layer between the conduction channel and the ferroelectric materials. Preferably, the buffer layer has only van der Waals interaction with both the conduction channel and the ferroelectric dielectric. Compared to interfaces with covalent bonding, the number of charge traps in the van der Waals interface is minimal. Such an ultrathin dielectric layer effectively blocks the electron (or hole) injection into the charge traps in the ferroelectric layer while not affecting the electric dipole gating effect. We expect that such interface engineering should restore the intrinsic switching behavior of 2D-FeFETs.

To prove the effectiveness of our method, we fabricated three devices from a single piece of FLBP crystal on BN substrates. These devices were numbered 2-1, 2-2, and 2-3. The schematic view and optical micrograph of the three devices are shown in Figure 3a. The schematic side view of a buffered device is shown in Figure 3b. In device 2-2, we use a piece of ultrathin BN crystal as the buffer dielectric between BP and P(VDF-TrFE) because the integrity of the BN crystal ensures simultaneously a low level of charge traps and a minimal number of pin holes at extremely small thicknesses. As a comparison, part of the same BP flake was fabricated into two unbuffered devices 2-1 and 2-3, which have direct contact with P(VDF-TrFE) (see Figure 3a). The thickness of the BP crystal, BN buffer layer, and bottom BN is approximately 10, 5, and 10 nm, respectively, as determined by AFM (see Figure 3c).

First, the behavior of devices 2-2 (with van der Waals buffer) and 2-3 (without van der Waals buffer) was studied by sweeping the nonferroelectric back gate V_{bg} before and after the P(VDF-TrFE) dielectric was fabricated on top of the FLBP. We found that the van der Waals buffer significantly reduces the number of populated charge traps in the device and preserves the mobility of the FLBP conducting channel, even in the case of zero voltage bias between the FLBP and the top (ferroelectric) gate electrode (details in the Supporting Information, section 4).

Second, the nonvolatile hysteretic $\sigma(V_{tg})$ curves of devices 2-1, 2-2, and 2-3 were examined. For device 2-2 (with van der Waals buffer), a pronounced (normal) hysteresis in $\sigma(V_{tg})$ was observed, with a bistable state at V_{tg} = 0 V (Figure 3d). The hysteretic behavior can be explained by the retarded dipole reversal of the P(VDF-TrFE) thin film, which is controlled by the top gate voltage.[40] The observed hysteresis character of device 2-2 was not affected by the top gate sweep rate when the sweep range $V_{tg\_max} > V_c \approx 22.5$ V (see details in Supporting Information, Figures S5 and S6). The memory window V_{Mem} is as large as 12.4 V (Figure 3d). The on/off ratio, defined as $\frac{\Delta\sigma}{\sigma} = \frac{(\sigma_{max} - \sigma_{min})}{\sigma_{min}}$ at V_{tg} = 0 V, is approximately 4100%, an order of magnitude larger than that in graphene.[17,40] The short blue line near V_{tg} = 0 V in Figure 3d is the sheet conductivity measured with a V_{tg} sweep range of ±0.5 V, after a 300 ms pulse polarization voltage of 40 or −40 V.

In stark contrast to device 2-2, unbuffered devices 2-1 and 2-3 showed anti-hysteresis behavior (Figure 3e), which is similar to what was observed in devices 1-1, 1-2, 1-3, and 1-4 as well as in many nonvolatile devices in the literature.[26,28,29] To further confirm our results, we fabricated another two groups of similar devices, and all devices with the van der Waals buffer demonstrated pronounced hysteresis behavior, while poor hysteresis or anti-hysteresis behavior were found in all devices that have direct BP-P(VDF-TrFE) interfaces (as shown in Supporting Information, Figure S7).

All the experimental results above provided consistent and strong evidence that the anti-hysteresis observed in BP-P(VDF-TrFE) 2D-FeFETs was caused by the electron traps presented in the P(VDF-TrFE) film. The ultrathin BN buffer layer works as a barrier, inhibiting the charge injection from the channel BP to the P(VDF-

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TrFE) layer while not affecting the dipole gating effect. We also noted interesting features in our data such that the value of the minimum conductance for forward and backward V_{tg} sweeps is different for the buffered devices (see Figure 3d and Figure S7). Such a phenomenon could be related to contact resistance being modified by the polarization of the ferroelectric layer. Detailed understanding of the contact effect would be an important topic to be studied in future works. We also noted that the apparent slopes at the electron side of the transfer curves for the buffered devices is generally lower than that of the unbuffered devices, which could be jointly influenced by the different location of V_{MB} as well as the continuous electron charging for the unbuffered device during the forward gate sweep at positive gate voltages.

Although anti-hysteretic FeFETs could in principle provide two logic states, the fairly long response time resulting from the charge trapping−detrapping mechanism and the unstable memory window V_{Mem} hampers its applications. Figure 4 shows the time-dependence of

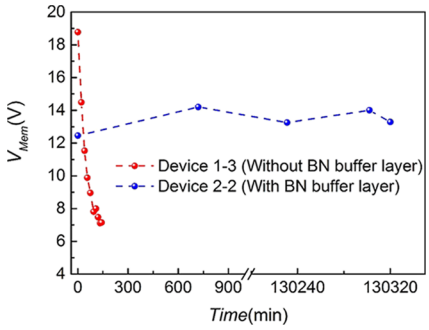

Figure 4. Stability of the memory window of buffered and unbuffered devices. The time-dependence of the memory window V_{Mem} for the unbuffered device 1-3 and the buffered device 2-2.

V_{Mem} for the unbuffered device 1-3 and the buffered device 2-2 when sweeping V_{tg} repeatedly with V_{tg_max} = 40 V. The stability of V_{Mem} for the buffered device is about 7000 times better than that for the unbuffered device. Here, the stability of V_{Mem} is expressed as $|\Delta V_{Mem}|_{max}/\Delta t$ where $|\Delta V_{Mem}|_{max}$ is the maximum variation of the memory window during the elapsed time Δt.

Figure 5a demonstrates the resistance state retention performance of device 2-2. The current of ON and OFF states (I_{ON} and I_{OFF}) were measured under a source−drain voltage of 5 mV, after a 300 ms pulse of V_{tg} = −40 V (ON state writing pulse) or V_{tg} = 40 V (OFF state writing pulse). The evolution of I_{ON} and I_{OFF} with time is plotted in the log−log scale in Figure 5a. It can be seen that after the V_{tg} pulse, both I_{ON} and I_{OFF} entered into asymptotic power-law relaxation with $I_{ON} \propto t^{-\alpha}$ and $I_{OFF} \propto t^{-\beta}$ (the red and blue dashed lines in Figure 5a) where the exponents $\alpha \approx 0.22$ and $\beta \approx 0.25$ indicate that both relaxations are rather slow and likely from the same origin. Such a slow power-law relaxation shows that the charge trap−detrapping process is negligible in our buffered device.[41] The mechanism behind the relaxation of I_{ON} and I_{OFF} is likely the depolarization in the ferroelectric dielectric observed in the literature.[42] It takes about 125 days for I_{ON} to decay to a value that is two times larger than the initial off current (see the highlighted arrow in Figure 5a), which is quite long, considering that our devices are not specifically optimized for a long retention time. In other words, without optimizing the pulse width, the thickness of the P(VDF-TrFE) layer, and the device area, we already have a 2D-FeFET that has fast program/erase speed and long retention time. This shows that BP-P(VDF-TrFE) FeFETs with the van der Waals buffer are very promising nonvolatile logic memory devices.

Figure 5b shows the bit writing process of device 2-2. To better visualize the bit writing process, we sweep V_{tg} and measure resistance ρ continuously. In practical operations, the bit writing can be completed with a simple pulse of V_{tg}. Basically, a short pulse of 40 V at V_{tg} can be used to write the 1 state from either the 0 or 1 initial state (Figure 5 b(i),(ii)), and a short pulse of −40 V at V_{tg} can be used to write 0 state from either the 0 or 1 initial state (Figure 5b(iii),(iv)).

RESULTS AND CONCLUSIONS

In conclusion, we have clarified the resistance switching mechanism for unbuffered BP-P(VDF-TrFE) 2D-FeFETs and have identified the dominating factor for the anti-hysteresis behavior to be the electron trapping in the P(VDF-TrFE) layer. We also developed a van der Waals buffer technique to eliminate the parasitic effect of these electron traps and to restore the intrinsic hysteresis behavior for the devices. Note that for 2D-FeFETs with PVDF P(VDF-TrFE) spin-coated on graphene, anti-hysteresis is rarely seen, which points to the possibility that the channel material might affect the properties (e.g., interfacial trap density) of the ferroelectric layer formed on the top. Our buffer method, in this regard, is a universal solution that provides normal hysteresis behavior independent of the type and number of charge traps inside the ferroelectric layer. This method should be broadly applicable to other 2D-FeFET systems and will be crucial in future technological

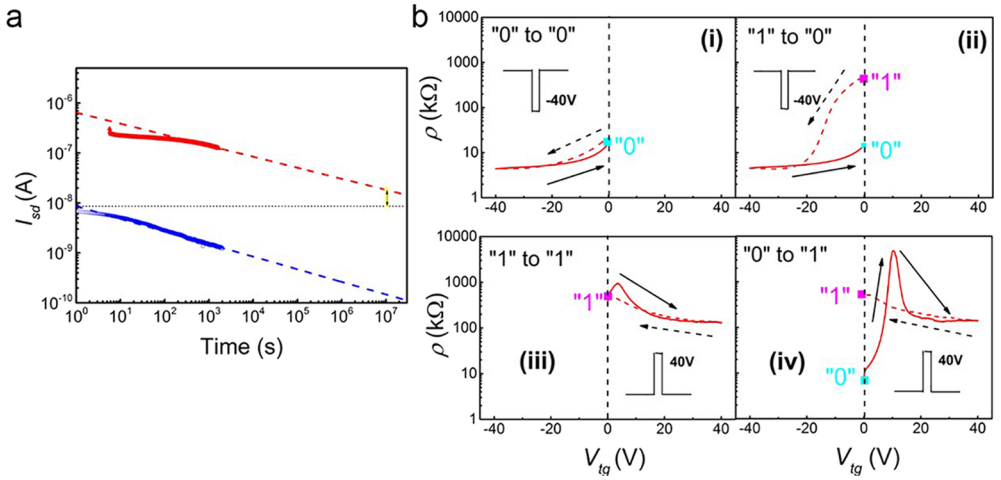

Figure 5. Retention test and logic operation of device 2-2. (a) Retention curves of device 2-2 after the application of 300 ms pulses of V_{tg} at ±40 V. I_{sd} was measured at V_{tg} = 0 V and V_{sd} = 5 mV. (b) Bit writing process of device 2-2. Writing "0" by a top gate voltage of −40 V from an initial state of 0 (Figure 5b(i)) and "1" (Figure 5b(ii)); writing 1 by a top gate voltage of 40 V from an initial state of 1 (Figure 5b(iii)) and 0 (Figure 5b(iv)).

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applications that aim to utilize the intrinsic properties of 2D-FeFETs for nonvolatile information storage and processing.

METHODS

The bulk BP crystals were grown by the same method mentioned in ref 13, and the BN crystals were grown by the method described in ref 43. FLBP, ultrathin BN crystals (for the buffer layer), and BN thin films (for the bottom gate substrate) were prepared by the mechanical exfoliation method.[44] The thicknesses of BP and BN were measured using AFM. The dry transfer method[45] was used to fabricate the (ultrathin top BN)/BP/(bottom BN) or BP/(bottom BN) van der Waals heterostructure, which was supported by 500 nm SiO_2/Si substrates. Standard e-beam lithography was used to pattern electrodes followed by an e-beam evaporation of Cr (6 nm) and Au (65 nm). The P(VDF-TrFE) (70:30 in mol %) thin film was spin-coated with a thickness of about 300 nm with the method described in ref 18. Top gate electrodes consisting of 15 nm-thick Al were deposited by e-beam evaporation or thermal evaporation with a shadow mask. The electrical measurements were performed in a probe station with devices in vacuum ($\sim 2 \times 10^{-5}$ mbar) at room temperature in a two-terminal configuration. A fixed source−drain voltage was applied using a Keithley 2400 source meter. Special attention has been given to protecting the BP flakes from being exposed to ambient conditions. All the sample preparation and device fabrication processes were done in vacuum, an inert atmosphere, or with the sample capped with a protection layer. The protection layer consists of a bilayer of 200 nm PMMA and 200 nm MMA or a layer of 300 nm P(VDF-TrFE) film. The memory window of FeFETs is defined as the threshold voltage shift of forward and backward gate sweeps,[46] and we use the hole side of the ambipolar curve throughout our manuscript for consistency. Threshold voltage can be determined by the constant current method: First, a "threshold current" value is defined; second, a constant bias voltage is applied to the device, and the gate voltage at which the source−drain current reaches the predefined threshold current is called the threshold voltage. To remove variation caused by sample dimension, we used a modified version of the definition in which a threshold conductance is set instead of a threshold current (0.1 μS is used, using other small values give a similar conclusion).[47]

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsami.9b15457.

AFM figures of device 1; ferroelectric polarization curve of the P(VDF-TrFE) thin film; schematic model of the charge trapping process in BP-P(VDF-TrFE) devices; behavior of devices 2-2 and 2-3 as tuned by V_{bg} with a normal dielectric; rate dependence of the hysteretic behavior of device 2-2; range dependence of the hysteretic behavior of device 2-2; and hysteretic behavior of devices 3 and 4 (PDF)

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Author Contributions

S.L.Y., Z.J.X., and J.-H.C. conceived the experiment. S.L.Y. and Z.J.X. fabricated the black phosphorus devices, performed transport measurements, and analyzed the data. H.H. and J.L.W. helped with the device fabrication and transport measurements. H.H. and J.L.W. provided the high-quality P(VDF-TrFE) solution and characterized the ferroelectric polarization of the P(VDF-TrFE) film. G.J.Y. and X.H.C. provided high-quality bulk black phosphorus crystals. T.T. and K.W. provided high-quality bulk BN crystals. S.L.Y., Z.J.X., X.-X.L., Z.H., X.H.C., J.L.W., and J.-H.C. discussed the results and analyzed the data. S.L.Y., Z.J.X. Z.H., and J.-H.C. wrote the manuscript, and all authors commented on it.

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Notes

The authors declare no competing financial interest.

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